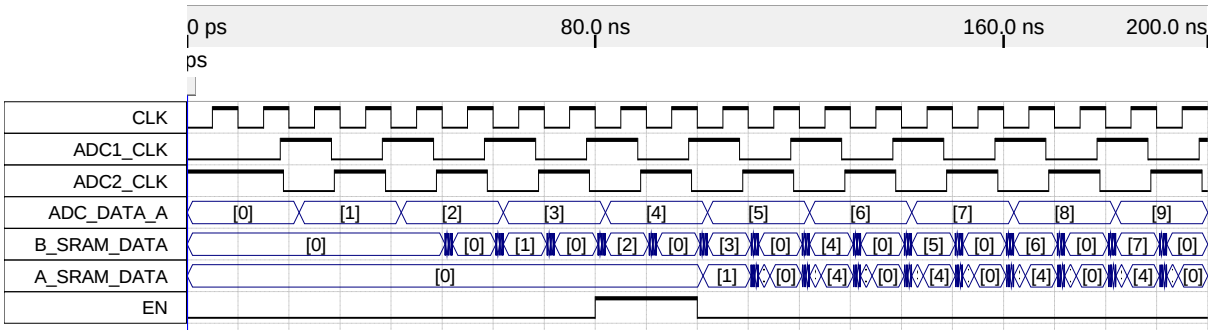
0 ps
80.0 ns
160.0 ns
200.0 ns
ps
CLK
ADC1_CLK
ADC2_CLK
ADC_DATA_A
B_SRAM_DATA
A_SRAM_DATA
EN
[0] [1] [2] [3] [4] [5] [6] [7] [8] [9]
[0] [0] [1] [0] [2] [0] [3] [0] [4] [0] [5] [0] [6] [0] [7] [0]
[0] [1] [0] [4] [0] [4] [0] [4] [0] [4] [0]